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The Silicon VerteX detector (SVX II) for the CDF experiment at the Tevatron $p\bar{p}$ collider is a 3-barrel 5-layer device with double-sided, AC-coupled silicon strip detectors. The readout is based on a custom IC, the SVX3 chip, capable of simultaneous acquisition, digitization and readout operation (dead-timeless). In this paper we report on the SVX II design and project status including mechanical design, frontend electronics, and data acquisition.

1. INTRODUCTION

The SVX II silicon vertex detector is part of the CDF II upgrade project, which will operate at the Fermilab Tevatron $p\bar{p}$ collider during Run II by early 2000. With the main injector upgrade of the Tevatron the instantaneous luminosity will be increased to $\sim 2\times10^{32}$ cm^{-2} s^{-1} with a bunch space crossing of 396 ns in the first phase of operation and, ultimately 132 ns in a second phase. The Tevatron center of mass energy will be increased from 1.8 TeV to 2.0 TeV and the expected integrated luminosity after the first years will be ~ 2 fb^{-1}. These parameters represent a step forward in the Tevatron operation compared to the past Run I achieved luminosities of $\sim 2\times10^{31}$ cm^{-2} s^{-1} with 3.5 μs bunch spacing. The guideline requirements for the SVX II design include a system with radiation hard frontend electronics to cope with the expected high radiation levels (0.5 MRad/fb^{-1} for the innermost SVX II layer) as well as capable of digitization and dead-timeless readout at the trigger level. Increased geometric coverage of the luminous region will provide track information up to pseudo-rapidities of $|\eta| < 2$. In addition, the detectors will be double-sided to provide improved pattern recognition and 3-D vertex reconstruction with impact parameter resolutions of $\sigma_\phi < 30$ μm and $\sigma_z < 60$ μm for central high momentum tracks.

The CDF silicon detector upgrade will include an additional device, the Intermediate Silicon Layers detector (ISL) [1], which will add more layers of silicon in the intermediate region between the SVX II and the new Central Outer Tracker (COT).

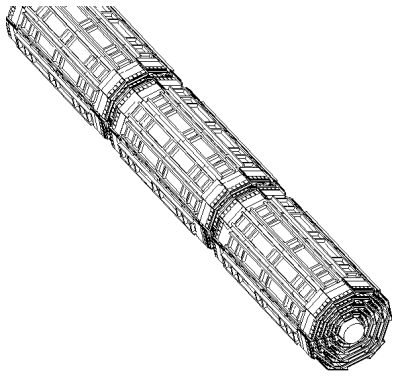

Figure 1. Schematic view of the 3 SVX II barrels.

2. SVXII MECHANICAL DESIGN

The SVX II is composed of 3 identical barrels, each 29 cm long, and located symmetrically around the nominal center of the detector. Figure 1 shows the barrel segmentation in 12 wedges, each spanning 30° in ϕ. There are 5 layers of silicon sensors per barrel, which are placed radially from 2.45 cm to 10.6 cm.

The basic structural unit of the SVX II detector is a ladder, which consist of 4 double-sided silicon microstrip sensors with width and strip multiplicity depending on the layer. Carbon fiber and

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Rohacell foam rails provide support to the ladder. A full ladder is readout from both ends through readout chips mounted on electrical hybrids on the surface of the silicon detectors. A schematic of a ladder end is shown in Figure 2. A printed circuit board called the Port Card (PC) located around the periphery of the barrel ends interfaces the hybrids and frontend chips with the rest of the readout data acquisition system. The ladders

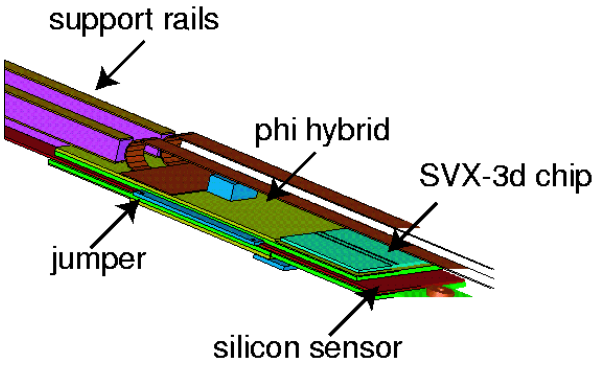

Figure 2. Schematic of an SVX II layer 0 ladder end. Only the ϕ-side is visible.

are supported and aligned on both ends by precision machined beryllium bulkheads. The bulkheads contain integrated cooling channels and are used also as heat sinks for the frontend electronics. The cooling system is designed to keep the silicon temperature less than $\sim 15^\circ$ C for nominal operating conditions and to prevent thermal runaway in the innermost layer at the maximum expected chip power dissipation for 2 fb^{-1} of delivered luminosity. The total SVX II heat load is 1.4 kW from the readout chips plus an additional 1.0 kW from the PCs. These requirements are met by flowing a 30% glycol/water mixture at a rate of $\sim$ 23 Kg/min. All power to the readout chips, silicon ladders and PCs will be provided by CAEN power supplies (one per wedge).

3. SILICON SENSORS

The silicon sensor layout is optimized to handle the high radiation levels and short integration times for the readout electronics while keeping good secondary vertex reconstruction and pattern recognition. All SVX II sensors are double-sided and are made from n-type high resistivity bulk silicon. Layers 0, 1 and 3 have 90° strips while layers 2 and 4 have small angle stereo ($\pm 1.2^\circ$) strips (see Table 1). The nominal thickness is 300 μm for the 90° stereo sensors and 275 μm for the small angle stereo. Strips are coupled to the readout electronics through integrated coupling capacitors formed by a thin insulating layer and an aluminum electrode. The 90° sensors are made by Hamamatsu Photonics using 4" silicon wafers and a double metal technology. To optimize the strip isolation on the ohmic side while minimizing the interstrip capacitance, a combination of individual and common p-stops has been used. The small angle detectors are manufactured by Micron Semiconductors using 6" silicon wafers. Table 1 shows a summary of mechanical properties of the SVX II sensors per layer. The total number of readout channels is 405,504 (211,968 on the p-side and 193,536 on the n-side).

In order to understand the effect of radiation on the SVX II sensors several of them were exposed to various levels of radiation and their performance studied on a beam test at Fermilab [2]. No decrease in signal size in the irradiated detectors with radiation doses up to 1.3 MRad were observed and the detectors made from 6" wafers had comparable performance to detectors from 4" wafers.

4. FRONTEND ELECTRONICS

The SVX II frontend electronics consists of a custom integrated circuit fabricated in the Honeywell radiation hard 0.8 μm bulk CMOS process called SVX3 chip [3]. An SVX3 chip set consist of a frontend (SVX3-FE) and a backend (SVX3-BE) and is shown schematically in Figure 3. The FE chip contains 128 channels, each with a charge integrator followed by an analog pipeline. The pipeline circuit consists of a switched array of 46 capacitors and a digital circuit shared by all channels called the skip logic which remove those cells from the pipeline which are flagged by external strobe signals. Up to 4 capacitors can be out of the loop. The BE chip

Table 1
Mechanical specifications of the SVX II sensors

Sensor parameters	Layer 0	Layer 1	Layer 2	Layer 3	Layer 4
Radial distance (cm)	2.45	4.67	7.02	8.72	10.6
Atereo angle (degrees)	90	90	+1.2	90	−1.2
$r\Phi$/z readout channels	256/512	384/576	640/640	768/512	896/896
$r\Phi$/z readout chips	2/2	3/3	5/5	6/4	7/7
$r\Phi$/z strip pitch (μm)	60/141	62/125.5	60/60	60/141	65/65
Total width (mm)	17.14	25.59	40.30	47.86	60.17
Total length (mm)	74.3	74.3	74.3	74.3	74.3

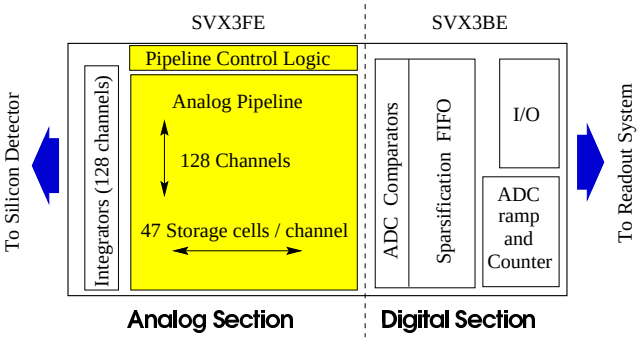

Figure 3. Schematic of the SVX3 readout chip. The approximate chip size is 6.26×12.0 mm^2.

contains 128 8-bit Wilkinson ADCs followed by a parallel-input serial-output memory with sparsification and differential current drivers for an 8-bit output bus. The SVX3 has the unique capability of continuous analog data acquisition during digitization and readout. This allows dead-timeless operation for Level 1 trigger rates up to 50 kHz. Two of the most critical specifications for the chip are the noise level and radiation hardness. Equivalent Noise Charge (ENC) levels have been measured to be 1700 for a typical sensor input capacitance of 20 pF. Radiation hardness has been demonstrated with irradiation tests carried out up to 4 MRad doses for various capacitance loads with acceptable performances [3].

The SVX3 chips are mounted on electrical hybrid packages made of printed thick film on beryllium oxide ceramic (BeO). The hybrids provide power and signal distribution to the chips as well as heat dissipation. A small silicon jumper glued to the edge of the sensor (see Figure 2) will route all connections between the ϕ and z hybrids through 100 μm diameter vias.

5. DATA ACQUISITION SYSTEM

A schematic of the whole data acquisition system for the SVX II detector is shown in Figure 4. Each SVX II wedge with 44 SVX3 chips is connected to single PCs through 5 Copper/Kapton laminate cables (one per layer) called High Density Interconnects (HDI). A basic feature of the PC is to convert the digital output of the SVX3 chips into optical signals through Dense Optical Interface Modules (DOIMs). There is a total of 5 DOIMs per PC, one for each layer of a wedge. Each DOIM drives a ribbon of optical fibers ($\sim$ 10 m length) at 53 MHz to VME crates with Fiber Interface Boards (FIBs) located on the side of the CDF detector. This highly parallel readout permits the entire detector to be readout in approximately 10 μs. The $r-\phi$ information is delivered to the Silicon Vertex Tracker (SVT), the SVX II Level 2 trigger processor, in the first 6 μs before the $r-z/\phi\prime$ information is readout. The SVT combines the SVX II Level 2 trigger data with the Level 1 tracking information from the central tracking chamber and computes track parameters (ϕ, p_T, and impact parameter d) with resolutions and efficiencies comparable to full offline analysis. Each FIB serializes the data from the low speed fiber system (DOIMs) into a high speed optical link (G-Link) operating at 1.5 GHz. The G-Links carry the data to VME Readout Buffer cards (VRBs) which hold the data until a Level 2 trigger decision is received. Upon a Level 2 accept signal the VRB sends the data to Level 3. The

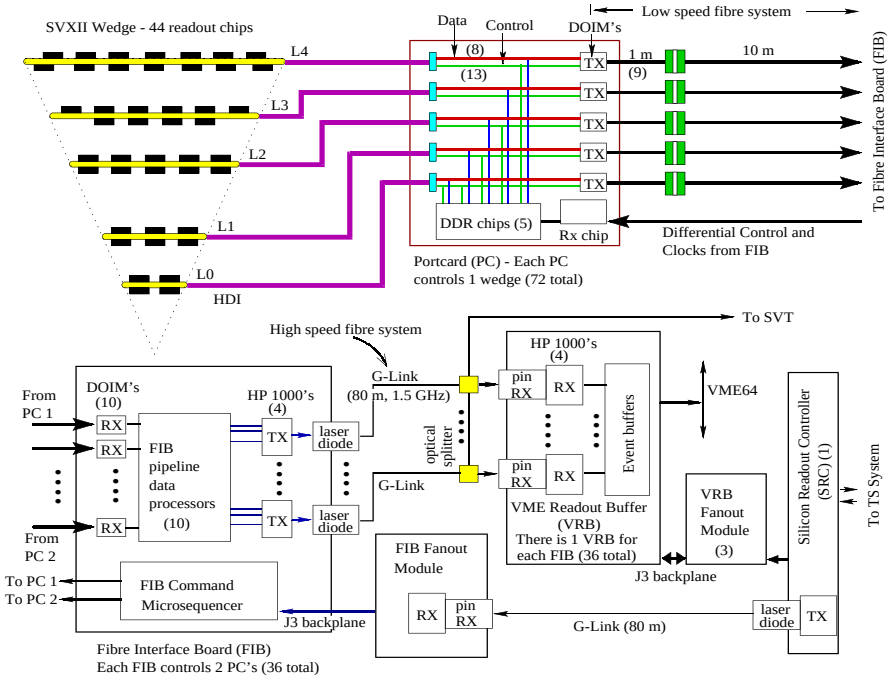

Figure 4. Schematic of the SVX II data aquisition system. The upper half shows the frontend readout (wedge and Port Card). The rest of the DAQ system is shown in the lower half. The FIB system is located in VME crates on the sides of the CDF detector, and the VRB and SRC systems are located further in the counting room.

master controller for the SVX II is the Silicon Readout Controller (SRC), which communicates with the CDF trigger supervisor.

6. CONCLUSIONS

The new CDF SVX II silicon vertex detector will provide, together with the ISL detector, standalone 3-D tracking and extended geometrical coverage increasing single track acceptances up to $|\eta| < 2$. The ability to use impact parameter information in the trigger to detect secondary vertices will substantially increase the physics reach of the CDF II detector. Applying impact parameter tracks at Level 2 will drastically increase the efficiency for heavy flavour physics processes, and reduce the large background rates expected in Higgs and new physics searches. The SVX II represents a new advance in the CDF history of building silicon detectors in challenging hadron collider environments. The excellent performance and experience gained in the construction of the Run I SVX and SVX' detectors will be essential for the SVX II project completion although the increase in the number of channels and the hostile new radiation environments will add, nevertheless, additional challenges during Run 2.

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